In the Specification

Please refer to the attached sheets reflecting changes to the specification.

On Page 1, under the heading "Related Applications," please replace the paragraph beginning at Line 2 with:

This application is related to:

U.S. Application No. 09/328,038 for a "HIGH AVAILABILITY LOCAL AREA NETWORK FOR A TELECOMMUNICATIONS DEVICE," filed June 8, 1999, now U.S. Patent No. 6,425,009;

U.S. Application No. 09/327,700 for a "TDM SWITCHING SYSTEM AND ASIC DEVICE," filed June 8, 1999, currently pending;

U.S. Application No. 09/327,971 for a "PROTECTION BUS AND METHOD FOR A TELECOMMUNICATIONS DEVICE," filed June 8, 1999, currently pending;

U.S. Application No. 09/328,173 for a "EVENT INITIATION BUS AND ASSOCIATED FAULT PROTECTION FOR A TELECOMMUNICATIONS DEVICE," filed June 8, 1999, now U.S. Patent No. 6,434,703;

U.S. Application No. 09/328,031 for a "FRAME SYNCHRONIZATION AND FAULT PROTECTION FOR A TELECOMMUNICATIONS DEVICE," filed June 8, 1999, currently pending;

U.S. Application No. 09/328,172 for a "TRANSITIONING A STANDARDS-BASED CARD INTO A HIGH AVAILABILITY BACKPLANE ENVIRONMENT," filed June 8, 1999, currently pending; and

U.S. Application No. 09/330,433 for a "CLOCK SYNCHRONIZATION AND FAULT PROTECTION FOR A TELECOMMUNICATIONS DEVICE," filed June 8, 1999, currently pending.

On Page 9, please replace the paragraph beginning at Line 3 with:

FIGURE 2 illustrates in further detail the components of switching unit 10. Service providers 14 communicate digital signals with each other using a backplane 20 that in a particular embodiment supports up to 16,384 time slots, corresponding to as many as 16,384 ports. In addition to control bus 16, switching unit controllers 12 and service providers 14 may be coupled to one another using a suitable combination of synchronization bus 22, power bus 24, reset bus 26, isolation bus 27, selection bus 28, and any other suitable

buses according to particular needs. In one embodiment, at least one input/output (I/O) module 32 is associated with each service provider 14 to support incoming and outgoing communications between service provider 14 and an associated network interface over associated link 34. A protection bus 30 couples I/O modules 32 and generally operates with control bus 16 and its associated physical layer protocol to provide protection switching and other capabilities desirable in avoiding a single point of failure and satisfying high availability requirements. Protection bus 30 is described more fully below with reference to FIGURE 6 and also in copending U.S. Application No. 09/327,971.

A2 cancel.

On Page 10, please replace the paragraph beginning at Line 11 with:

In one embodiment, redundancy in connection with control bus 16 may apply to the physical transport media but not necessarily to the link layer and physical control devices. For example, as shown in FIGURE 3, a single controller 38 may be used in connection with duplicate control links 40a and 40b, duplicate data links 42a and 42b, and a transmission path through transmit buffer 48 and receive buffer 49 to support redundant "A" and "B" control buses 16. In response to a failure, controller 38 and the control of transmit and receive buffers 48 and 49, respectively, may be electrically isolated from other switching unit controllers 12 and service providers 14 according to a suitable isolation technique involving isolation bus 27 or otherwise. This helps to prevent a single point of failure from propagating within system 8 and helps to satisfy high availability requirements. Suitable isolation techniques involving isolation bus 27 are described more fully in U.S. Patent No. 6,434,703.

A3

On Page 14, please replace the paragraph beginning at Line 24 with:

Switching unit controllers 12 and service providers 14 desiring to communicate message packet 50 using control bus 16 each use some or all of arbitration code 54 to determine which competing sender will win the arbitration cycle corresponding to a particular transfer cycle and therefore be allowed to communicate message packet 50 within that transfer cycle. An arbitration cycle may begin any time control bus 16 is deemed idle, as discussed more fully below with reference to FIGURE 7B. In one embodiment, an arbitration cycle is performed even if only one sender desires use of control bus 16. Within the arbitration cycle, the sender having the highest message priority according to priority code 70 is awarded use of control bus 16 for the associated transfer cycle. If multiple senders have message packet 50 with the same priority code 70, then control bus 16 is awarded to the sender having the highest physical priority according to sender address 74. A sender that has been awarded use of control bus 16 as a result of the arbitration cycle may be referred to as the bus master for the associated transfer cycle, while all other cards including any losing senders may be referred to as slaves for the transfer cycle.

A4

On Page 19, please replace the paragraph beginning at Line 22 with:

Because bus snooping allows one or more cards, one or more particular service providers 14 for example, to monitor message packets 50 destined for one or more other cards, destination codes 80 and receive codes 90 help support 1+1, N+1, N+X, and other suitable redundancy schemes often desirable in avoiding a single point of failure and satisfying high availability requirements. For example, receive code 90 for a redundant protection card 14 may be configured to allow the protection card 14 to snoop on or otherwise receive some or all message packets 50 destined for any protected cards 14 within a specified protection group. If one of the protected cards 14 fails, the protection card 14 may be informed of the failure and seamlessly assume at least some of the responsibilities of the failed protected card 14 until the failed protected card 14 can be replaced, repaired, or otherwise returned to service. One or more exemplary protection techniques involving bus 30 are described more fully in copending U.S. Application No. 09/327,971.

On Page 21, please replace the paragraph beginning at Line 14 with:

SYS_CLK signal 110 is the common system clock that one or more switching unit controllers 12 drive during operation of switching unit 10 and that determines the timing of all transfers on control bus 16. In one embodiment, the clock is redundant, having an "A" and "B" pair, and software associated with switching unit 10 determines which "A" or "B" clock is to be used at any given time. In a particular embodiment, the clock operates at 8MHz, although the present invention contemplates any appropriate clock speed. Preferably, each switching unit controller 12 and service provider 14 will use a self-generated clock that is phase and frequency locked to the system clock rather than using the system clock directly. One or more ASIC devices associated with each switching unit controller 12 and service provider 14 may be used to generate such a synchronized clock. Clock synchronization within switching unit 10 is described more fully in copending U.S. Application No. 09/330,433. Exemplary ASIC devices capable of providing such clock synchronization are described more fully in copending U.S. Application No. 09/327,700.